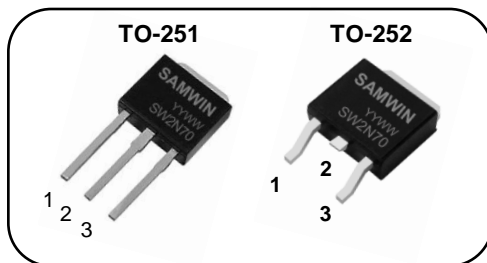


N-channel MOSFET

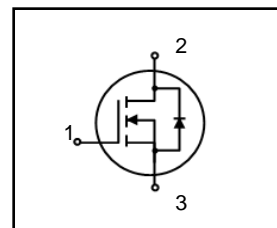
Features

- High ruggedness
- $R_{DS(ON)}$ (Max 7 Ω) @ $V_{GS}=10V$
- Gate Charge (Max 5nC)
- Improved dv/dt Capability
- 100% Avalanche Tested



1. Gate 2. Drain 3. Source

BV_{DSS}	: 700V
I_D	: 2A
$R_{DS(ON)}$: 7ohm



General Description

This power MOSFET is produced with advanced VDMOS technology of SAMWIN. This technology enable power MOSFET to have better characteristics, such as fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics. This power MOSFET is usually used at AC adaptors and SMPS.

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW I 2N70	SW2N70	TO-251	TUBE
2	SW D 2N70	SW2N70	TO-252	REEL

Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	700	V
I_D	Continuous Drain Current (@ $T_C=25^\circ C$)	2.0	A
	Continuous Drain Current (@ $T_C=100^\circ C$)	1.3	A
I_{DM}	Drain current pulsed (note 1)	8.0	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single pulsed Avalanche Energy (note 2)	140	mJ
E_{AR}	Repetitive Avalanche Energy (note 1)	2.8	mJ
dv/dt	Peak diode Recovery dv/dt (note 3)	4.5	V/ns
P_D	Total power dissipation (@ $T_C=25^\circ C$)	28	W
	Derating Factor above 25°C	0.22	W/°C
T_{STG}, T_J	Operating Junction Temperature & Storage Temperature	-55 ~ + 150	°C
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.	300	°C

Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thCS}	Thermal resistance, Junction to Lead Max	40	°C/W
R_{thJA}	Thermal resistance, Junction to ambient	62.5	°C/W

Electrical characteristic ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	$V_{GS}=0V, I_D=250\mu A$	700	-	-	V
I_{DSS}	Drain to source leakage current	$V_{DS}=700V, V_{GS}=0V$	-	0.4	1	μA
		$V_{DS}=560V, T_C=125^\circ\text{C}$	-	-	100	μA
I_{GSS}	Gate to source leakage current, forward	$V_{GS}=30V, V_{DS}=0V$	-	-	100	nA
	Gate to source leakage current, reverse	$V_{GS}=-30V, V_{DS}=0V$	-	-	-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	-	4.0	V
$R_{DS(ON)}$	Drain to source on state resistance	$V_{GS}=10V, I_D = 1.0A$	-	5.0	7.0	Ω
Dynamic characteristics						
C_{ISS}	Input capacitance	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$	-	450	530	pF
C_{OSS}	Output capacitance		-	45	50	
C_{RSS}	Reverse transfer capacitance		-	9	10	
$t_{d(on)}$	Turn on delay time	$V_{DS}=350V, I_D=2A, R_G=25\Omega$	-	-	55	ns
t_r	Rising time		-	-	90	
$t_{d(off)}$	Turn off delay time		-	-	100	
t_f	Fall time		-	-	70	
Q_g	Total gate charge	$V_{DS}=560V, V_{GS}=10V, I_D=2A$	-	15.1	21	nC
Q_{gs}	Gate-source charge		-	2.2	3	
Q_{gd}	Gate-drain charge		-	4.4	6	

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	-	-	2.0	A
I_{SM}	Pulsed source current		-	-	8.0	A
V_{SD}	Diode forward voltage drop.	$I_S=2A, V_{GS}=0V$	-	-	1.4	V
T_{rr}	Reverse recovery time	$I_S=2A, V_{GS}=0V,$	-	260	-	ns
Q_{rr}	Breakdown voltage temperature	$di_f/dt=100\mu A/\mu s$	-	1.09	-	μC

※. Notes

1. Repeitative rating : pulse width limited by junction temperature.
2. $L = 95\text{mH}, I_{AS} = 0.5A, V_{DD} = 50V, R_G=25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 0.5A, di/dt = 300A/\mu s, V_{DD} \leq BV_{DSS}, \text{Starting } T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

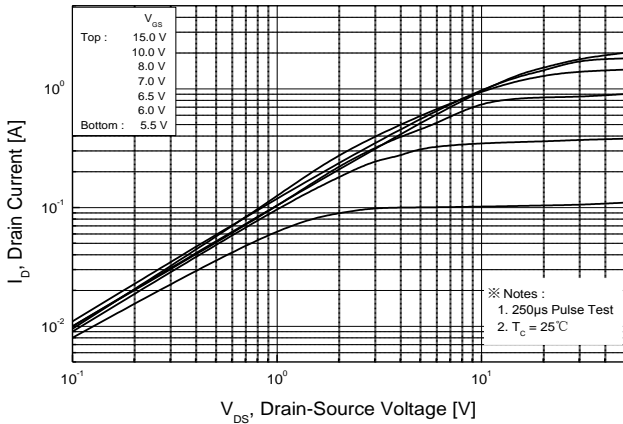


Fig. 2. Transfer characteristics

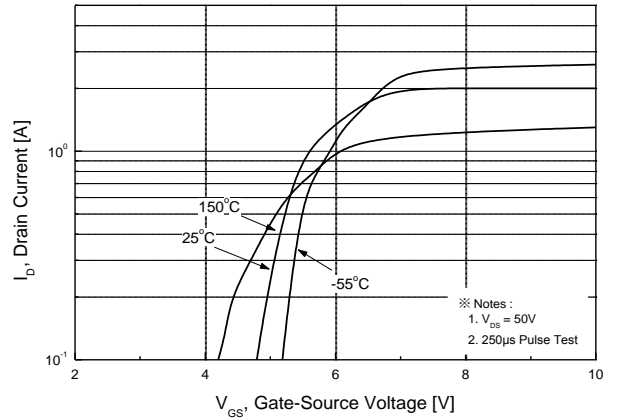


Fig. 3. On-resistance variation vs. drain current and gate voltage

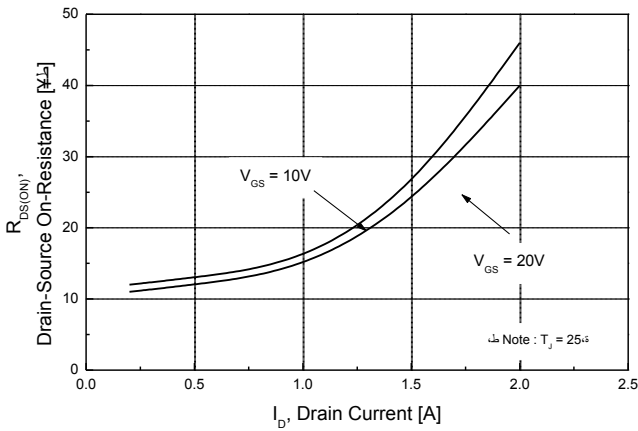


Fig. 4. On state current vs. diode forward voltage

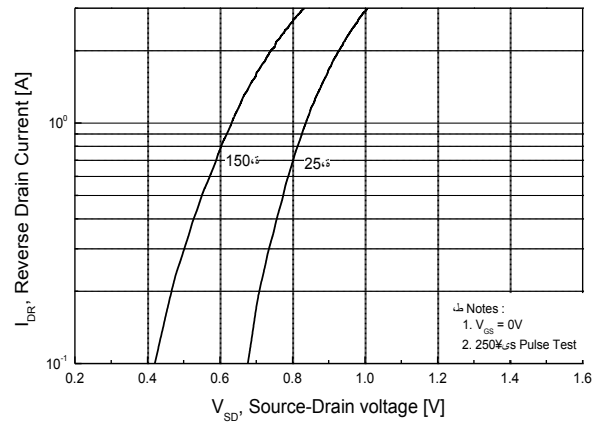


Fig. 5. Capacitance characteristics (Non-Repetitive)

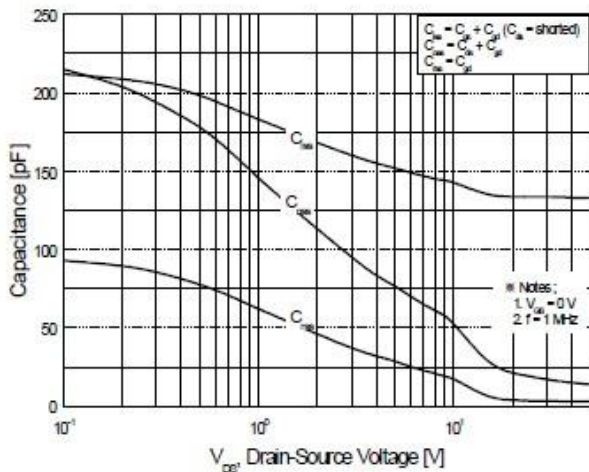


Fig. 6. Gate charge characteristics

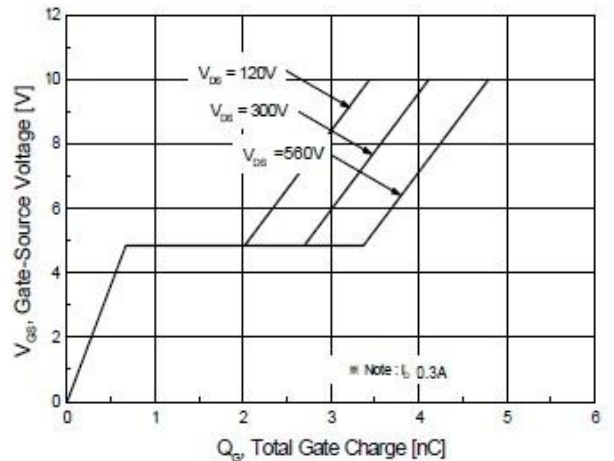


Fig 7. Breakdown Voltage Variation vs. Junction Temperature

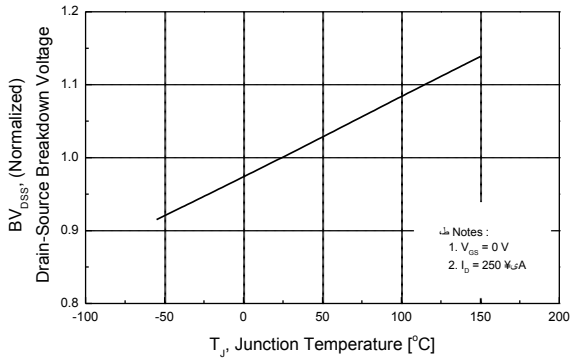


Fig. 8. On resistance variation vs. junction temperature

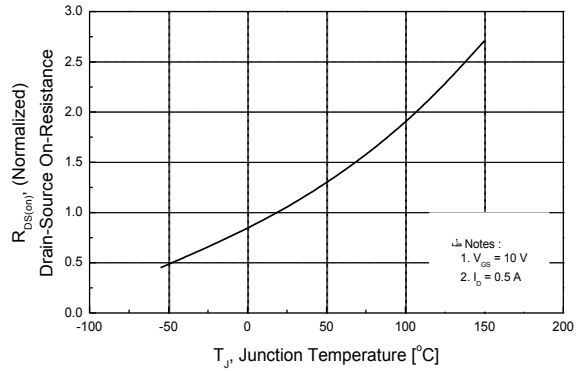


Fig. 9. Maximum drain current vs. case temperature.

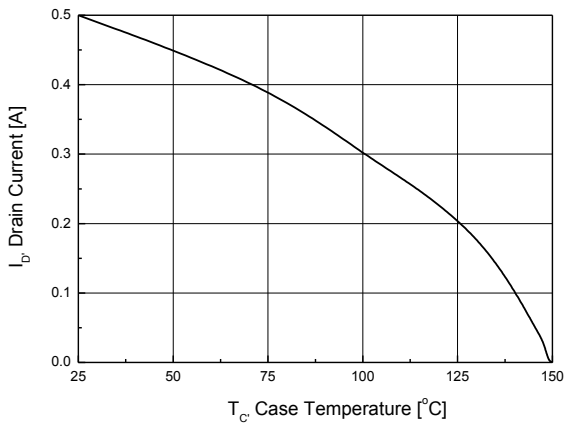


Fig. 10. Maximum safe operating area

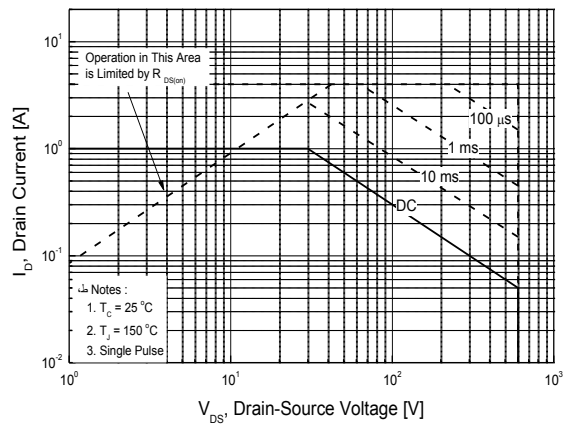


Fig. 11. Transient thermal response curve

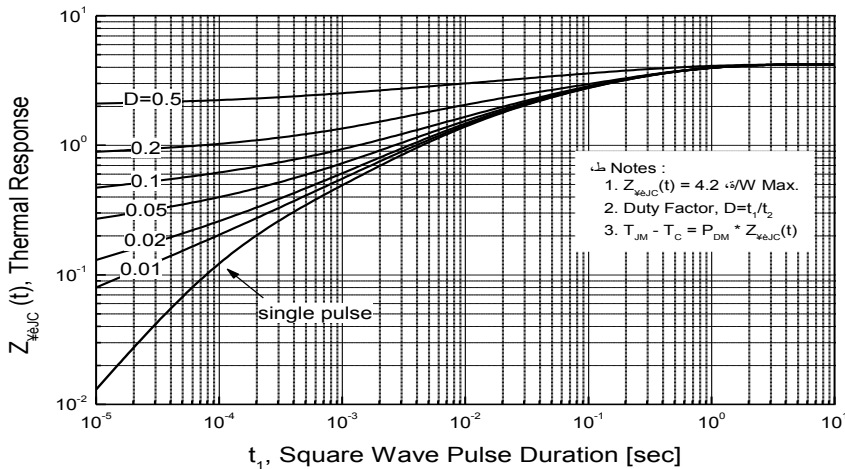


Fig. 12. Gate charge test circuit & waveform

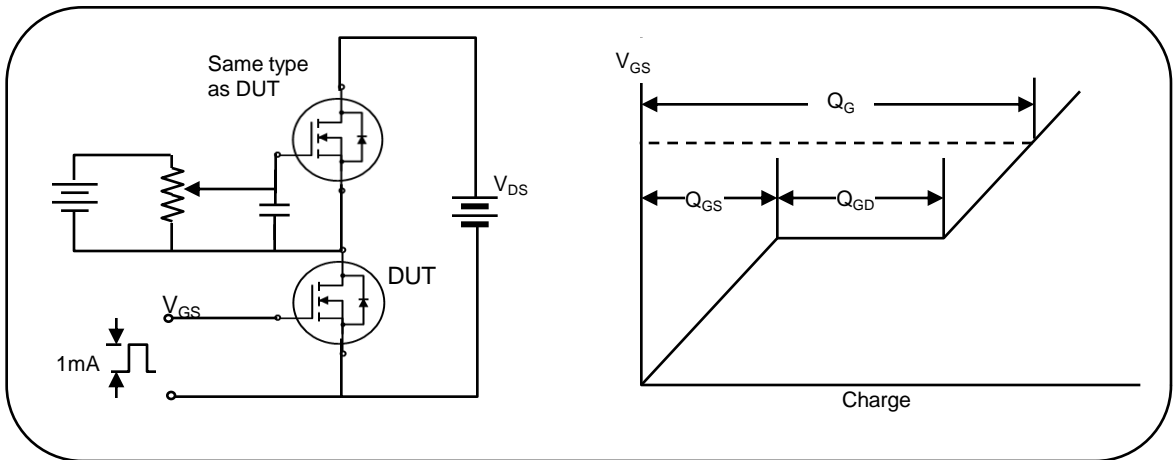


Fig. 13. Switching time test circuit & waveform

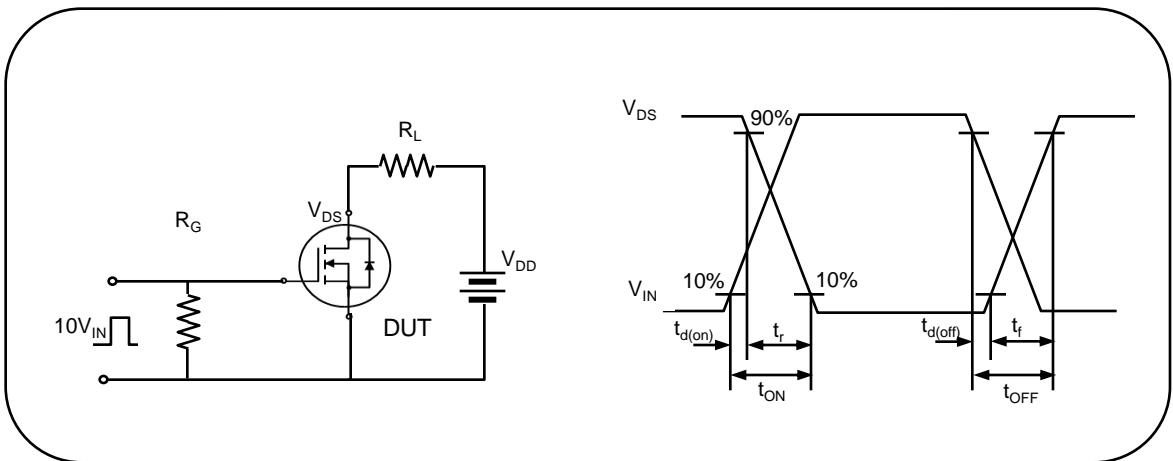


Fig. 14. Unclamped Inductive switching test circuit & waveform

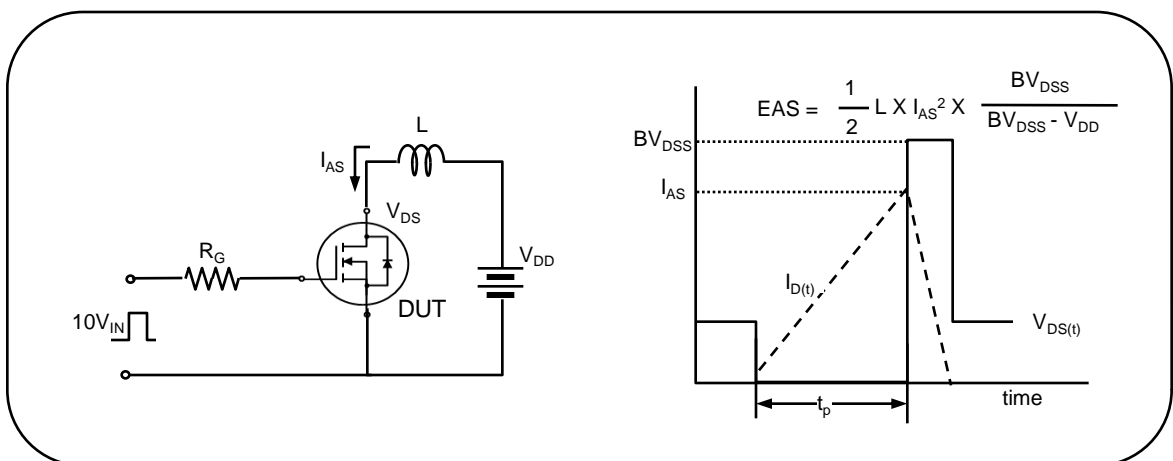
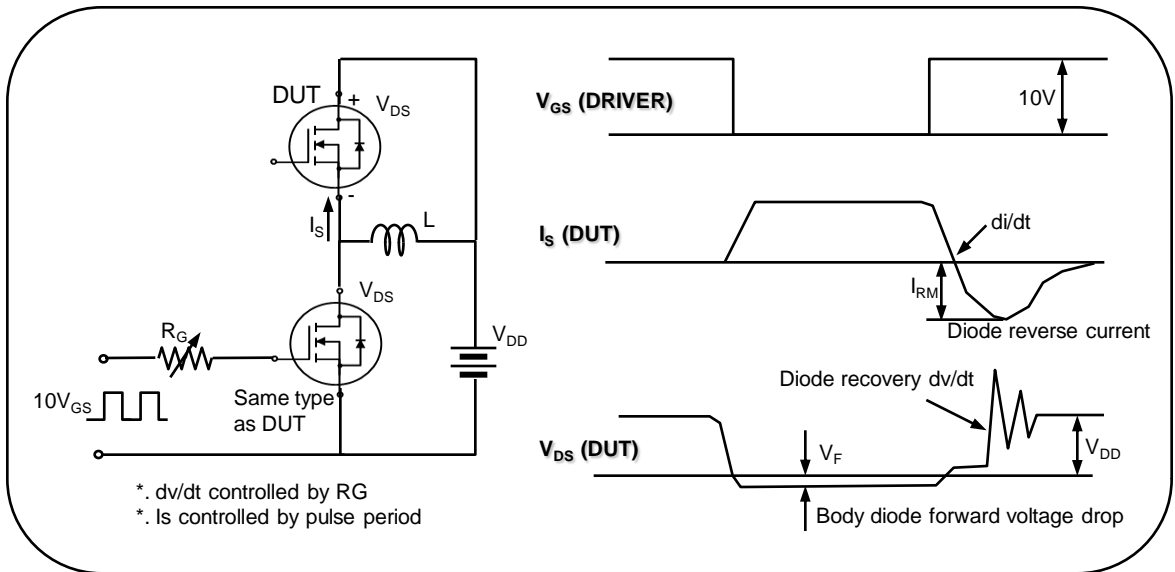


Fig. 15. Peak diode recovery dv/dt test circuit & waveform



REVISION HISTORY

Revision No.	Changed Characteristics	Responsible	Date	Issuer
REV 1.0	Origination, First Release	Alice Nie	2009.12.12	XZQ
REV 2.0	Updated the format of datasheet and added Order Codes.	Alice Nie	2011.04.28	XZQ

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